

In re Patent Application of
SERGIO ET AL.
Serial No. 09/994,384
Filed: NOVEMBER 26, 2001

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application. By this amendment, independent Claims 8, 11, 15, 19 and 22 have been amended to further clarify features of the present invention. Claims 8-24 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

The claimed invention is directed to a method and a system for reading a capacitive sensor that overcomes the various problems of conventional approaches as discussed in the background section of the present application. More precisely, as set forth in independent Claim 8, for example, the invention includes reading a capacitive sensor including an array of capacitors ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other. A biasing and reading circuit having column and row selectors is used, and a charge amplifier outputs a voltage of the capacitance of a selected capacitor of the array. The approach includes resetting an output voltage of the charge amplifier, connecting nonselected row and column lines of the array to a reference voltage while connecting one of an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier, and applying a step voltage on the

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capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state.

II. The Claims are Patentable

Claims 8-24 were rejected in view of Zhang (US Patent No. 5,847,599) taken alone or in combination with Smisko for the reasons set forth on pages 2-8 of the Office Action. Applicants contend that Claims 8-24 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

Independent Claim 8 is directed to a method for reading a capacitive sensor comprising an array of capacitors ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each other, using a biasing and reading circuit comprising column and row selectors, and a charge amplifier outputting a voltage of the capacitance of a selected capacitor of the array. The method includes resetting an output voltage of the charge amplifier, connecting nonselected row and column lines of the array to a reference voltage while connecting one of an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier, and applying a step voltage on the capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state.

Independent method Claim 11 includes providing a biasing and reading circuit comprising column and row selectors, an amplifier, connected to the column and row selectors, for outputting a voltage of the capacitance of a selected capacitor of the array, and an auxiliary capacitor connected to the column and row selectors. The method includes connecting nonselected rows and columns of the array to a reference voltage while connecting one of the auxiliary capacitor and the selected capacitor as an input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier, and applying a step voltage on the capacitor that is connected on the input of the amplifier and reading the output voltage at steady-state.

Also, independent Claim 15 is directed to a system for reading a capacitive sensor comprising an array of capacitors connected in rows and columns. The system includes a biasing and reading circuit comprising an amplifier for outputting a voltage representing the capacitance of a selected capacitor, an auxiliary capacitor, configuration switches for coupling one of the auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier, and an analog-to-digital converter for converting the output voltage to digital data. Also included is an input interface circuit for connecting deselected row lines and column lines of the array to a reference voltage and while coupling the selected

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capacitor of the capacitive sensor to the biasing and reading circuit, a microprocessor for performing noise filtering and real-time correction of data, and a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor.

Independent Claim 19 is directed to an integrated circuit for reading a capacitive sensor comprising an array of capacitors connected in rows and columns. The circuit includes: column and row selectors; an amplifier, connected to the column and row selectors, for outputting a voltage of the capacitance of a selected capacitor of the array; an auxiliary capacitor connected to the column and row selectors; configuration switches for connecting deselected row lines and column lines of the array to a reference voltage and while coupling one of the auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier; and a controller for controlling the configuration switches.

And, independent Claim 22 is directed to a capacitive sensor device comprising: an array of capacitors connected in rows and columns; and a reading circuit for reading the array of capacitors and comprising column and row selectors, an amplifier, connected to the column and row selectors, for outputting a voltage of the capacitance of a selected capacitor of the array, an auxiliary capacitor connected to the column and row selectors, configuration

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switches for connecting deselected row lines and column lines of the array to a reference voltage and while coupling one of the auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier, and a controller for controlling the configuration switches.

It is these combinations of features which are not fairly taught or suggested in the cited references and which patentably define over the cited references.

The Examiner has relied on the Zhang patent as allegedly disclosing each and every feature of the claimed invention as set forth in Claims 8-14. Zhang discloses an amplifier for use in a MOS sensing array of an imaging device, and is concerned with performing the "amplification as quickly as possible" (Col. 3, lines 10-14). The amplifier includes an operational amplifier and a feedback capacitor. During an equalization period, the voltage between the output of the operational amplifier and the inverting input is equalized. During an amplification period, an input signal is applied and amplified by the combination of the operational amplifier and the feedback capacitor. Additionally, during the amplification period, the compensation capacitor of the operational amplifier is disabled.

Firstly, Applicants maintain that the Examiner has misinterpreted the cited reference. Specifically, Applicants note that in Zhang there is no discussion of connecting nonselected row and column lines of the array to a reference

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voltage while connecting one of an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier. Indeed, although the circuit of Zhang includes the use of a feedback capacitor (Fig. 2), there is no teaching of connection of nonselected sensor capacitors to a reference voltage while connecting the feedback capacitor and selected capacitor to the amplifier as claimed.

By this amendment, the independent Claims 8, 11, 15, 19 and 22 were amended to emphasize this distinction between the present invention and the circuit of Zhang.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

The Smisko reference was relied upon by the Examiner for teaching the use of an A/D converter, an input interface circuit and a microprocessor with respect to Claims 15-24. More specifically, Smisko discloses a method and apparatus for reducing noise in a light sensing circuit having a photodiode array coupled to a charge amplifier through a field effect transistor transfer switch. Thermal noise generated by the transfer switch is combined with image signals inputted to the charge amplifier resulting in an outputted noisy image signal. The Smisko approach takes two consecutive readings of the charge amplifier output, one before and one after closing the

transfer switch and after opening it. The thermal noise generated by the transfer switch, and added to the next reading of the charge amplifier output, is equal to the difference between these two readings. Once stored, this difference can be subtracted from the previously mentioned "next reading", resulting in the elimination of this noise term.

Again, nothing in this reference teaches connecting nonselected row and column lines of the array to a reference voltage while connecting one of an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier, as claimed. Accordingly, the Smisko reference cannot make up for the deficiencies of the Zhang reference as discussed above.

As the Examiner is aware, to establish a prima facie case of obviousness, the prior art reference must teach or suggest all the claim features. Both the suggestion to make the claimed combination and the reasonable expectation of success must be founded in the prior art and not in Applicants' disclosure.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 8, 11, 15, 19 and 22. Furthermore, no proper modification of the

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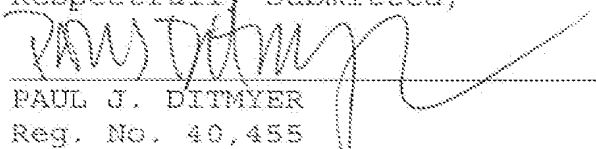
teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102 and §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone to resolve such informalities.

Respectfully submitted,



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